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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,160	07/25/2001	Toshiharu Yanagida	09792909-5171	7228

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EXAMINER

IM, JUNGHWA M

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 11/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/915,160

Applicant(s)

YANAGIDA, TOSHIHARU

Examiner

Junghwa M. Im

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2,5,6 and 25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2,5,6 and 25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Claim Objections***

Claim 2 is objected to because of the following informalities.

Claim 2 recites the dependency on claim 1 which is cancelled. However, for examining purpose, Examiner assumes that claim 2 is dependent on claim 25 which is the sole independent claim.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 5, 6 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (US 6,333,206), hereafter Ito, in view of Nishikawa et al. (US 5,878,943), hereafter Nishikawa, and Milewski et al. (US 6,330,967), hereafter Milewski and Andros et al. (US 5,633,533), hereafter Andros.

Regarding claims 2, 5, 6 and 25, Figure 28 of Ito shows a semiconductor apparatus comprising: a semiconductor chip 3 inherently having a circuit pattern; a plurality of solder bumps 2 of two different materials on the semiconductor chip connect to the circuit pattern, the solder bumps forming spaces; a resin film 10 disposed on the semiconductor chip and said solder

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bumps, said resin film being disposed in the spaces between solder bumps such that upper surfaces of said solder bumps protrude from said resin layer; and a mounting board 1.

Ito does not teach the metal bumps made of two different materials and a precoated land with a solder layer. Starting on column 5, lines 29, Ito shows a variety of materials for solder balls, and Figure 5A of Milewski shows in detail solder bumps are made of two different material, a high melting ball 35, and a eutectic solder layer 39. It would have been obvious to one of ordinary skill in the art to modify the metal bumps of Ito with the teaching of Milewski in order to improve the connection between a package and a supporting substrate.

And regarding the aspect of a precoated land with a solder layer, Figure 4 of Milewski teaches a eutectic coated lands 51 (col. 2, lines 65-68) aligned with the solder bumps (Fig. 5A) on the mounting board 21. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Milewski in to the device of Ito in order to have precoated lands with eutectic layer on a mounting board since precoated lands enhances the attachment of chips to a mounting board.

The combined teaching of Ito and Milewski fail to show the aspect of cleaning the metal bumps. Figure 18 of Nishikawa shows in the surfaces of the metal bumps being cleaned (col.12, lines 18-25). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Nishikawa to the device of Ito and Milewski in order to enhance the strength of the soldered junction through having a clean surface of metal bumps.

The device with combined teachings of Ito, Milewski and Nishikawa is substantially identical except a gap formation between the resin layer and the mounting board. Figure 6 of Andros shows a semiconductor device with a gap formation between the resin layer (51; col.5,

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lines 25-27) and the board (27). It would have been obvious to one of ordinary skill in the art to modify the layer of the resin formation in the device of Ito, Milewski and Nishikawa with the teaching of Andros for the protection of the semiconductor device only.

In addition, a different embodiment (Figure 13) of Ito also shows spacing between a resin formation (18 or 13 on the chip) and the board (13).

Regarding claim 2, Nishikawa teaches the surfaces of the metal bumps being cleaned of components causing a rise of a connection resistance and a drop in a joint strength at least connection interfaces. Nishikawa teaches, throughout the specification especially in col. 1, lines 22-40, cleaning method of oxide/contamination coating on the surface of metal bumps to enhance better alignment between the soldering joint.

### ***Response to Arguments***

Applicant's arguments with respect to claims the pending claims have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie c. Lee can be reached on (703) 308-1690. The fax phone numbers for the

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organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmi  
November 17, 2003

A handwritten signature in black ink, appearing to read 'Eddie Lee', with a large, sweeping initial 'E'.

EDDIE LEE  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800